Wideband Scalable Electrical Model for Microwave/Millimeter Wave Flip Chip Interconnects

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***Abstract*—We present a method for developing fully scalable lumped element models for flip chip interconnects. Measurements of test structures and full wave simulations are used to generate circuit models for various single bump configurations. Furthermore, regression models are developed for scaling the values of the elements with the physical attributes of the circuit. First, the method is validated using only two factors, then the model is extended to more inputs related to the bump geometry and placement. The values of L and C in a simple π model have been scaled with the conductor overlap, the distance from the ground bump to the edge of the ground plane, the width of the CPW launch, the bump height and diameter. Explicit formulas are obtained for L and C as a function of those variables. It has been found that the value of the inductance varies with the conductor overlap, bump height and diameter, while the capacitance is mostly affected by conductor overlap. This paper presents the first fully scalable model for microwave flip chip technology.**

***Index Terms*—Flip-chip, lumped element model, regression model, scalable model.**

I. INTRODUCTION

THE vertical interconnect solutions, both for level-one (flip chip) and level-two (ball grid array), have been considered in the past few years for RF and microwave applications. The flip chip structures have the advantages of reduced size and weight, compatibility with automatic manufacturing and minimized electrical path to the motherboard. Therefore, the modeling and characterization of flip chip packages to microwave frequencies is of great practical interest.

The equivalent lumped element model of the bump transition is very important in understanding and predicting the electrical behavior of the flip chip assembly and essential for design rule development. The variation of the physical attributes of the flip chip assembly has to be reflected in the values of the elements of the circuit. Previous work shows variation with bump height [1], diameter [2], and conductor overlap [3], but there is no work showing the variation of the lumped elements with more than one factor at a time and that can be extended to a comprehensive model for design rule development. The approach presented in this paper allows this goal to be achieved. First, only two factors, the conductor overlap (o) and the distance from the ground bump to the edge of the ground plane (d), have been included to validate the approach. By including all the other factors involved in the design process [4], the first fully scalable model for microwave flip chip has been developed. In addition to o and d, the final model includes variation with bump height, bump diameter and CPW launch signal width, and the experiment is based on finite element method (FEM) [5] and circuit simulations.

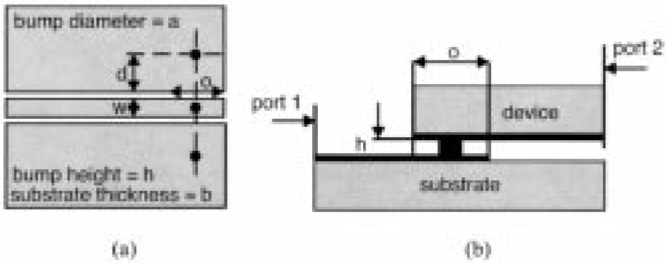

Fig. 1. Basic flip chip configuration: (a) transmission line and bump geometry parameters and (b) side view of simulated structure.

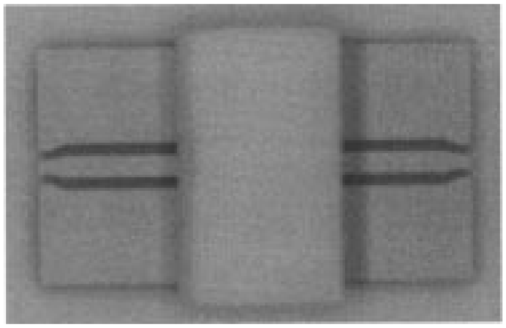

Fig. 2. Top view of fabricated test structure.

II. APPROACH

Coplanar waveguide is the transmission line of choice when designing a flip chip transition. The main advantage is the elimination of ground vias, easier manufacturing and fewer sources of mismatch and package resonances [6]. In order to develop the approach for lumped element model extraction and scaling for the flip chip transition, test structures have been fabricated to mount a 50 Ω alumina coplanar waveguide (CPW) on an alumina board. The substrate thickness is 10 mil and the dielectric constant 9.6. The thermosonic attachment process uses the ball bond from a wirebond and a combination of heat, pressure and ultrasonic energy to form a bond between the bump and the metallization on the joining surface. The resulting bumps are 70 μm in diameter and 25 μm in height. Fig. 1 shows a schematic of the simulated flip chip assembly indicating all the factors included in the two experiments. Fig. 2 shows a top view picture of a fabricated flip chip test structure.

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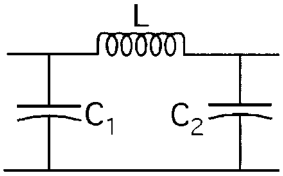


Fig. 3. Lumped element model of flip chip transition.

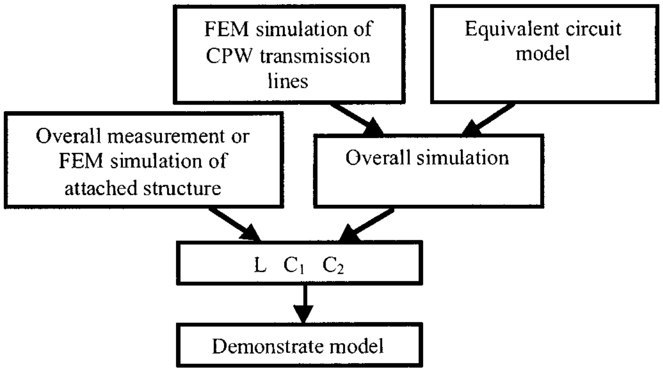


Fig. 4. De-embedding technique used to extract inductance and capacitance values.

TABLE I
TESTED GEOMETRIES AND RESULTING PARASITIC VALUES

Run #	*o* (μm)	*d* (μm)	L (pH)	C (fF)
1	120	50	10	15.5
2	120	200	10	15
3	200	50	17.5	20.5
4	200	200	17.5	20.5

TABLE II
VARIABLES AND ANALYSIS INTERVALS FOR EXTENDED MODEL

Variable	"-" level	"+" level
Bump height *h*	20 μm	100 μm
Bump diameter *d*	30 μm	100 μm
CPW width *w*	150 μm	250 μm
Distance from ground bump to the edge of the ground plane *d*	25 μm	100 μm
Conductor overlap *o*	150 μm	300 μm

TABLE III
EXPERIMENT AND EXTRACTED LUMPED ELEMENT VALUES

Run #	*h*	*a*	*w*	*d*	*o*	L(pH)	C(fF)
1	-	-	-	-	+	90	43
2	+	-	-	-	-	90	33
3	-	+	-	-	-	50	24
4	+	+	-	-	+	100	53
5	-	-	+	-	-	72	25
6	+	-	+	-	+	130	48
7	-	+	+	-	+	90	42
8	+	+	+	-	-	75	28
9	-	-	-	+	-	63	25
10	+	-	-	+	+	110	47
11	-	+	-	+	+	82	42
12	+	+	-	+	-	72	30
13	-	-	+	+	+	80	38
14	+	-	+	+	-	87	24
15	-	+	+	+	-	38	20
16	+	+	+	+	+	95	45

The study of the reflection due to the ball interconnect is done using the equivalent circuit model in Fig. 3, which is similar to the configuration for the flip-chip transition in [2]. C_1 denotes the discontinuity capacitance at the chip, C_2 the discontinuity capacitance at the substrate and L the inductance. No resistive losses and a symmetrical model $(C_1 = C_2 = C)$ were assumed for this case. Since the transition includes the three ground-signal-ground bumps, the lumped elements in the model reflect the whole transition rather than the bump itself, accounting for all the phenomena occurring in the interconnection area.

The approach for de-embedding the effect of the interconnection is presented in Fig. 4. The values of the lumped elements are obtained by matching the measured or simulated S-parameters of the overall attached structure to the cascaded CPW transmission lines and bump model. The measurements are performed using HP8510B network analyzer with on-wafer ground-signal-ground probes. All structures are measured with 150 μm wide pitch probes. The network analyzer is calibrated using a line-reflect-match (LRM) [7] technique.

Several test structures have been fabricated and measured, containing all the combinations of the two input variables o and d and resulting in a simple factorial experiment [8]. Table I shows the values of the two variables for the four combinations. By applying the method presented above, the values of the capacitors C and inductor L in the model have been extracted for each of the four cases. The values of L and C are shown in the last two columns of Table I. An interesting result is the variation of the inductance in the model with the overlap. This shows that the model does not account only for the bump geometry, but for all the parasitic modes and the overall behavior of the transition.

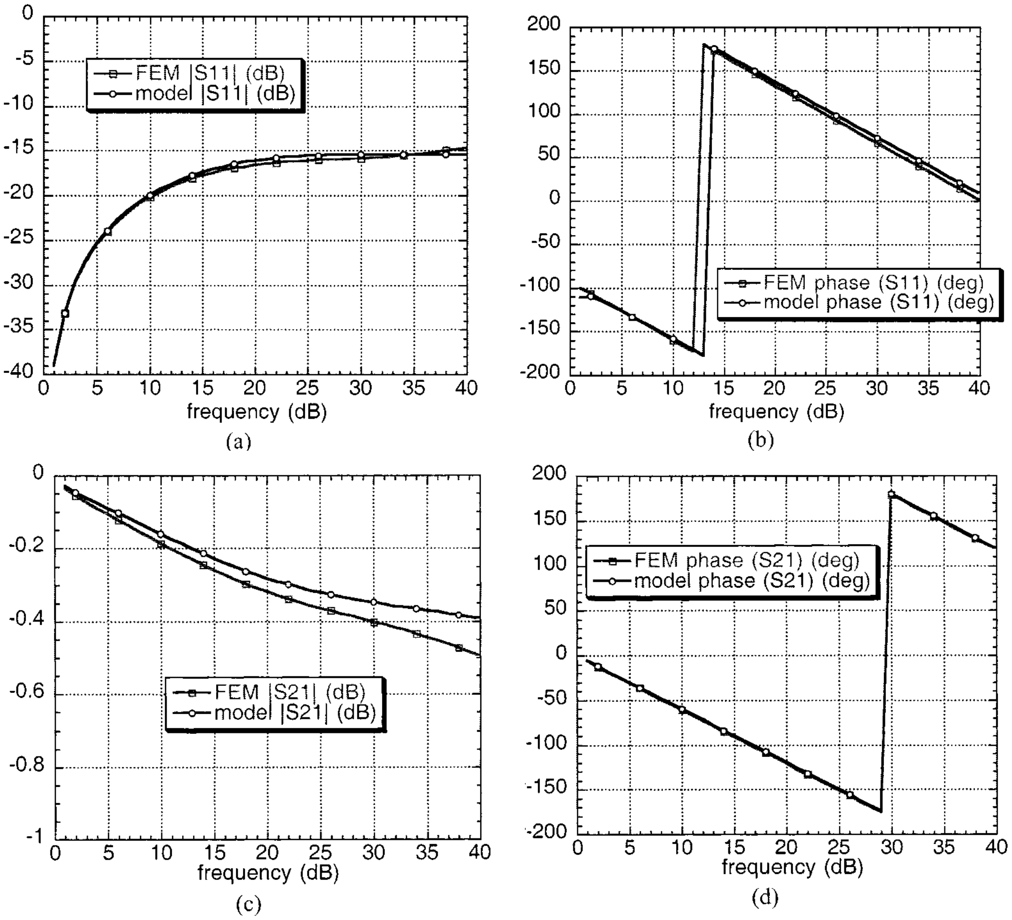
A. Model Scaling

The need for fully scalability of the model can be satisfied by developing regression models [8] for L and C based on the data in Table I. The general expressions are

$$\hat{L} = \beta_0 + \beta_1 \cdot o + \beta_2 \cdot d + \beta_{12} \cdot o \cdot d$$
$$\hat{C} = \alpha_0 + \alpha_1 \cdot o + \alpha_2 \cdot d + \alpha_{12} \cdot o \cdot d \quad (1)$$

where the coefficients α and β are derived from the effects of the two variables and the interaction between them [8]. The calculations resulted in

$$\hat{L}(\text{pH}) = -1.25 + 0.094 \cdot o\ (\mu\text{m})$$
$$\hat{C}(\text{fF}) = 7.35 + 0.066 \cdot o\ (\mu\text{m}). \quad (2)$$



(a) (b) (c) (d)

Fig. 5. Comparison between FEM and simulated performance including lumped element model for run #1: (a) S_{11} magnitude, (b) S_{11} phase, (c) S_{21} magnitude, and (d) S_{21} phase.

The effect of d and the interaction between o and d are very small compared with o; therefore d has been neglected. The linearity of the statistical model in the 120 μm to 500 μm interval for the overlap has been demonstrated in [4] and justifies the choice of a linear regression. This model allows the designer to predict the value of the lumped elements in the model as a direct function of the design inputs. The conclusions are valid in the specified intervals for the input variables and the model has been extended to more factors involved in the basic design process, resulting in the first fully scalable lumped element model for microwave flip chip.

III. EXTENDED SCALABLE MODEL

The extended model includes the factors related to the basic bump geometry, placement and transmission line launch configuration, as presented in [4]. The five factors are bump height h, bump diameter a, conductor overlap o, distance from ground bump to the edge of the ground plane d and coplanar waveguide signal line width w. The summary of the factors and the analysis intervals are presented in Table II. The fabrication process discussed in the previous section did not allow variation with bump height and diameter, therefore the remaining experiment is based on FEM and circuit simulations only.

The schematic of the simulated structure is presented in Fig. 1(b). A 2^{5-1} partial factorial design [8] has been chosen for the 5 variables. The experiment consists of $2^{5-1} = 16$ treatment combinations. The values of L and C in the model have been extracted following the same approach in Fig. 4, using an overall FEM simulation instead of measurements. The experiment and the results for all the 16 treatment combinations are presented in Table III.

The model verification includes the comparison of the overall FEM simulation with the circuit simulation including the developed model. The magnitude and phase results for S_{11} and S_{21} are presented in Fig. 5 for run #1. The same good agreement has been obtained for the rest of the runs.

The values of the regression coefficients have been extracted and applied to the general model including main effects and one level interactions

$$\begin{aligned}\hat{L} = {} & \beta_0 + \beta_1 \cdot h + \beta_2 \cdot a + \beta_3 \cdot w + \beta_4 \cdot d \\ & + \beta_5 \cdot o + \beta_{12} \cdot h \cdot a + \beta_{13} \cdot h \cdot w \\ & + \beta_{14} \cdot h \cdot d + \beta_{15} \cdot h \cdot o + \beta_{23} \cdot a \cdot w \\ & + \beta_{24} \cdot a \cdot d + \beta_{25} \cdot a \cdot o + \beta_{34} \cdot w \cdot d \\ & + \beta_{35} \cdot w \cdot o + \beta_{45} \cdot d \cdot o \\ \hat{C} = {} & \alpha_0 + \alpha_1 \cdot h + \alpha_2 \cdot a + \alpha_3 \cdot w + \alpha_4 \cdot d \\ & + \alpha_5 \cdot o + \alpha_{12} \cdot h \cdot a + \alpha_{13} \cdot h \cdot w \\ & + \alpha_{14} \cdot h \cdot d + \alpha_{15} \cdot h \cdot o + \alpha_{23} \cdot a \cdot w \\ & + \alpha_{24} \cdot a \cdot d + \alpha_{25} \cdot a \cdot o + \alpha_{34} \cdot w \cdot d \\ & + \alpha_{35} \cdot w \cdot o + \alpha_{45} \cdot d \cdot o.\end{aligned} \tag{3}$$

The normal probability plot [8] of the effects for L indicated that the significant factors are h, a, d, o and the wd interaction. Similarly, the significant factors for the C expression are h, w, d, o and the ha, aw, ad, wo and do interactions. After translating the variables from coded units ($+1$ and -1) to their real values, the following expressions have been obtained for L and C estimates:

$$\begin{aligned}\hat{L}(\text{pH}) = {} & 31.37 + 0.2 \cdot h\,(\mu\text{m}) - 0.29 \cdot a\,(\mu\text{m}) \\ & + 0.06 \cdot w\,(\mu\text{m}) + 0.24 \cdot d\,(\mu\text{m}) \\ & + 0.2 \cdot o\,(\mu\text{m}) - 0.0018 \cdot w\,(\mu\text{m}) \cdot d\,(\mu\text{m}) \\ & + 0.0011 \cdot a\,(\mu\text{m}) \cdot d\,(\mu\text{m}) \qquad (4) \\ \hat{C}(\text{fF}) = {} & 18.86 + 0.01 \cdot h\,(\mu\text{m}) - 0.18 \cdot a\,(\mu\text{m}) \\ & - 0.05 \cdot w\,(\mu\text{m}) - 0.07 \cdot d\,(\mu\text{m}) \\ & + 0.18 \cdot o\,(\mu\text{m}) + 0.0008 \cdot h\,(\mu\text{m}) \cdot a\,(\mu\text{m}) \\ & + .0003 \cdot a\,(\mu\text{m}) \cdot w\,(\mu\text{m}) \\ & + 0.0007 \cdot a\,(\mu\text{m}) \cdot d\,(\mu\text{m}) \\ & - 0.0001 \cdot w\,(\mu\text{m}) \cdot o\,(\mu\text{m}) \\ & - 0.0003 \cdot d\,(\mu\text{m}) \cdot o\,(\mu\text{m}).\end{aligned}$$

As expected, the conductor overlap is the most significant factor, followed in order by bump height, diameter, coplanar waveguide signal width and distance from ground bump to the edge of the ground plane. This result agrees with the conclusions obtained in [4]. The bump height and diameter affect the inductance more, while the capacitance is mostly affected by the conductor overlap. The strong dependence of the inductance on o is explained by the increased length of transmission line within the transition for higher overlap values. Also, the signs of the terms in the regression model show how the respective factors affect the lumped element values. For example, the inductance increases with higher and thinner bumps and larger overlaps. The capacitance increases with the overlap, too. All these facts prove that the model not only accounts for the bumps, but for all the phenomena occurring in the interconnection area.

IV. CONCLUSION

A novel approach for scaling the elements of the equivalent circuit of a flip chip transition has been presented. The method is based on extracting the lumped element values with a hybrid method including measurements and/or simulations then developing regression models for the specified intervals of the input variables. The factors considered are the bump height, diameter, CPW signal line width, conductor overlap, and the distance from the ground bump to the edge of the ground plane. A fractional factorial experiment has been designed and the values of L and C have been extracted for all the treatment combinations. Then, regression models have been applied to these values and explicit formulas for L and C as a function of the design inputs have been developed. The models show strong variation with o for C and variation with o, h and a for L. A new result is the dependence of L with the overlap, counting for the increased transmission line length in the interconnection area for larger overlaps. The method is very flexible and it has been demonstrated that it can be extended to any factors in any intervals. Based on this, the first fully scalable lumped element model for microwave flip chip has been demonstrated for developing design rules and technical insight for flip chip interconnections at RF and microwave frequencies.

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