Wideband Scaleable Electrical Model for Microwave/Millimeter Wave Flip Chip Interconnects

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Abstract

We present an original method for developing fully scaleable lumped element models for flip chip interconnects. Measurements of test structures and full wave simulations are used to generate circuit models for various single bump configurations. Furthermore, regression models are developed for scaling the values of the elements with the physical attributes of the circuit. The values of L and C in a simple π model have been scaled with the conductor overlap (*o*) and the distance from the ground bump to the edge of the ground plane (*d*). It has been found that high overlaps have not only an increased capacitive effect, but an inductive one also and that there is no variation in the lumped element values with *d*. By incorporating all the factors involved in the flip chip design, the first comprehensive fully scaleable model for microwave flip chip technology will be developed based on this approach.

1. Introduction

The vertical interconnect solutions, both for level-1 (flip chip) and level-2 (ball grid array) have been considered in the past few years for RF and microwave applications. The flip chip structures have the advantages of reduced size and weight, compatibility with automatic manufacturing and minimized electrical path to the motherboard. Therefore, the modeling and characterization of flip chip packages to microwave frequencies is of great practical interest.

The equivalent lumped element model of the bump transition is very important in understanding and predicting the electrical behavior of the flip chip assembly and essential for design rule development. The variation of the physical attributes of the flip chip assembly has to be reflected in the values of the elements of the circuit. Previous work shows variation with bump height [1], diameter [2], and conductor overlap [3], but there is no work showing the variation of the lumped elements with more than one factor at a time and that can be extended to a comprehensive model for design rule development. The approach presented in this paper allows this goal to be achieved. Only two factors, the conductor overlap (*o*) and the distance from the ground bump to the edge of the ground plane (*d*) have been included to validate the approach. By including all the other factors involved in the design process [4], the first fully scaleable model for microwave flip chip will be developed.

2. Approach

In order to develop the lumped element model for the flip chip transition, test structures have been fabricated to mount an alumina coplanar waveguide (CPW) on an alumina board. The substrate thickness is 10 mil. The thermosonic attachment process uses the ball bond from a wirebond and a

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combination of heat, pressure and ultrasonic energy to form a bond between the bump and the metallization on the joining surface. The resulting bumps are 70 μm in diameter and 25 μm in height. Figure 1 shows a schematic and a side picture of the attached assembly.

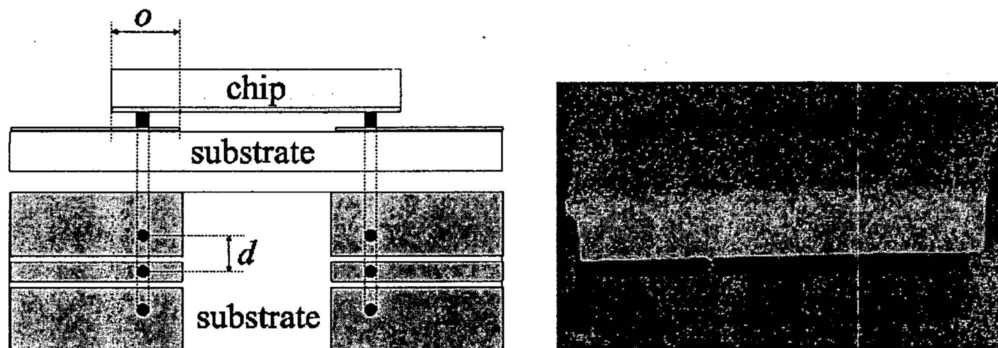

Figure 1. Schematic and side picture of the attached assembly

The study of the reflection due to the ball interconnect is done using the equivalent circuit model in Figure 2, which is similar to the configuration for the flip-chip transition in [2]. C_1 denotes the discontinuity capacitance at the chip, C_2 the discontinuity capacitance at the substrate and L the inductance. Symmetrical model has been assumed for this case (C_1=C_2). Since the transition includes the three ground-signal-ground bumps, the lumped elements in the model reflect the whole transition rather than the bump itself, accounting for all the phenomena occurring in the interconnection area.

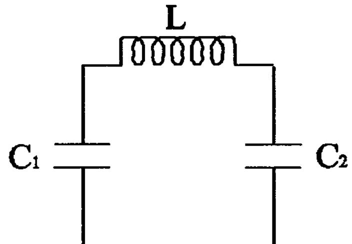

Figure 2. Lumped element model

The approach for de-embedding the effect of the interconnection is presented in Figure 3. The values of the lumped elements are obtained by matching the measured S-parameters of the overall attached structure to the cascaded CPW transmission lines and bump model.

Several test structures have been fabricated and measured, containing all the combinations of the two input variables *o* and *d* and resulting in a simple factorial experiment [5]. Table 1 shows the values of the two variables for the four combinations. By applying the method presented above, the values of the capacitors C and inductor L in the model have been extracted for the four cases. The values of L and C are shown in the last two columns of Table 1. An interesting result is the variation of the inductance in the model with the overlap. This shows that the model does not account only for the bump geometry, but for all the parasitic modes and the overall behavior of the transition.

The verification of the model accuracy is presented in Figure 4 for the Run # 3. All the other three runs show the same very good agreement.

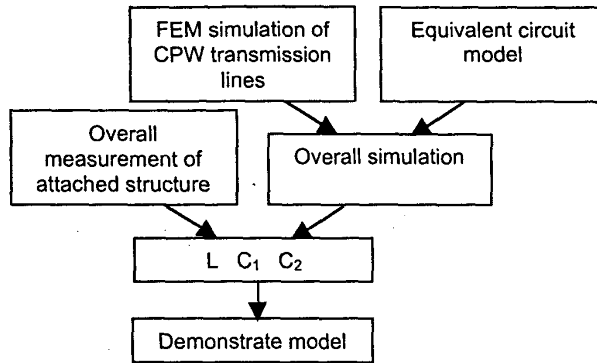

Figure 3. De-embedding technique

Run #	*o* (μm)	*d* (μm)	L (pH)	C (fF)
1	120	50	10	15.5
2	120	200	10	15
3	200	50	17.5	20.5
4	200	200	17.5	20.5

Table 1. Experiment

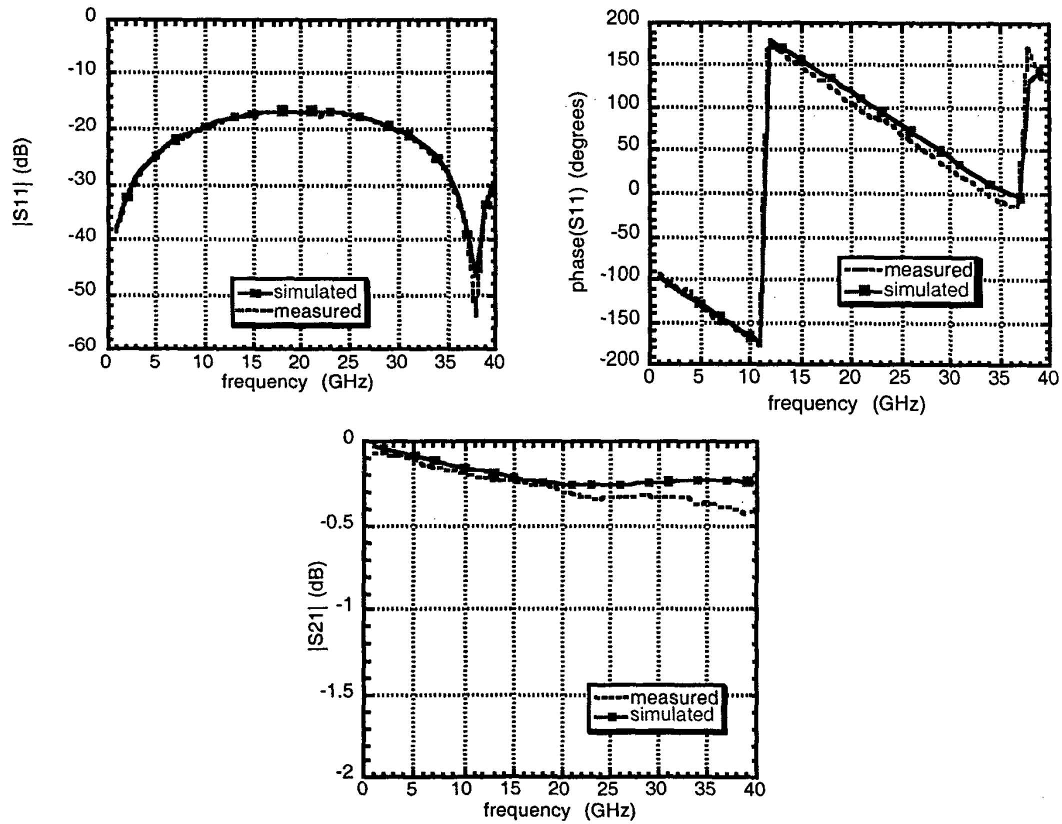

Figure 4. Model verification for run #3

3. Model scaling

The need of fully scalability of the model can be satisfied by developing regression models [5] for L and C based on the data in Table 1. The general expressions are

$$\hat{L} = \beta_0 + \beta_1 \cdot o + \beta_2 \cdot d + \beta_{12} \cdot o \cdot d$$

$$\hat{C} = \alpha_0 + \alpha_1 \cdot o + \alpha_2 \cdot d + \alpha_{12} \cdot o \cdot d$$

where the coefficients α and β are derived from the effects of the two variables and the interaction between them [5]. The calculations resulted in the followings:

$$\hat{L}(pH) = -1.25 + 0.094 \cdot o(\mu m)$$

$$\hat{C}(fF) = 7.35 + 0.066 \cdot o(\mu m)$$

The effect of *d* and of the interaction between *o* and *d* are very small compared with *o* therefore have been neglected. The linearity of the statistical model in the 120 μm to 500 μm interval for the overlap has been demonstrated in [4] and justifies the choice of a linear regression. Also, the result is in accordance with the analytical analysis presented in [4], which concluded that the conductor overlap is a very important design factor to consider in a flip chip assembly. This model allows the designer to predict the value of the lumped elements in the model as a direct function of the design inputs. The result is valid in the specified interval for the input variables and can be extended to all the factors involved in the design process in any desired interval for comprehensive design rule development.

4. Conclusion

A novel approach for scaling the elements of the equivalent circuit of a flip chip transition has been presented. The method is based on extracting the lumped element values with a hybrid method including measurements and simulations, then develop regression models for the specified intervals of the input variables. Considering the conductor overlap (*o*) and the distance from the ground bump to the edge of the ground plane (*d*), explicit formulas for L and C in the lumped element model have been developed They show strong variation with *o* and no variation with *d*. A new result is the dependence of L with the overlap, counting for the parasitic effects in the interconnection area. The method is very flexible and can be extended to all the factors involved in the flip chip design, for any specified intervals. Based on this, the first comprehensive, fully scalable lumped element model for microwave flip chip will be demonstrated, for developing design rules and technical insight for flip chip interconnections at RF and microwave frequencies.

References:

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