

# Design Rule Development for Microwave Flip Chip Applications

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## Abstract

This paper presents a novel approach for analysis of factors to be considered when designing a flip chip package. It includes the design of an experiment and statistical analysis of the outputs. The most significant factors are found to be, from most to least important, the length of the area where the device and the substrate overlap (referred to as conductor overlap), the bump diameter and the width of the coplanar waveguide transmission line launch. These results are valid for conductor overlaps between 300 and 500  $\mu\text{m}$ . For a lower overlap value (120  $\mu\text{m}$ ), the bump height becomes significant also. The substrate thickness in the 10 to 25 mil interval is found to be statistically insignificant, therefore it can be eliminated from further analysis.

## 1. Introduction

Along with the recent advances in microwave and millimeter wave system development, the choice of the interconnection solutions has become a very important issue, since the performance of the system is determined in part by the interconnection geometry. The vertical interconnect solutions, both for level-1 (flip chip) and level-2 (ball grid array) have been considered in the past few years. For microwave circuit applications, low cost, high density and short transition interconnect are considered to be the main advantages of the flip chip technique. Since it gained attention as a potential interconnection solution for microwave and millimeter wave applications, the flip chip technology has been electrically, mechanically and thermally analyzed for understanding its advantages and limitations [1]. The factors that affect the electrical performance of a flip chip interconnection have been established and their importance studied. They include the bump height [2], bump horizontal diameter [3], and conductor overlap [4]. The next step is to gain a general understanding of all the involved factors, their relative importance and the interaction between them. The design of experiments method presented in this paper allows these goals to be achieved.

## 2. Fractional factorial design

Experiments are performed by investigators in virtually all fields of inquiry, to discover something about an unknown phenomenon or system [5]. A designed experiment is a series of tests in which a set of input variables are purposely changed so that the experimenter can observe and identify the reasons for changes in the output response. If the experiment is correctly conducted, valid and objective conclusions are obtained for the system. The most complete strategy when dealing with several factors is a full factorial experiment. Commonly used factorial designs are the

$2^k$ , with  $k$  independent variables each at two levels, widely used in factor screening experiments. The effect of a factor is defined as the change in response produced by the change in the level of the factor. In some experiments it can be found that the difference in response between the levels of a factor is not the same at all levels of the other factors. When this occurs, there is an interaction between the factors. All the results of such an experiment are valid only for the specified interval of each variable.

If the volume of the factorial experiment is too large and the experimenter can assume that certain high order interactions are negligible, the information on the main effects and two-order interactions can be obtained by running only a fraction of the full factorial experiment. This is called fractional factorial design and this is the strategy adopted for the flip-chip analysis being presented in this paper.

### 3. Experiment

For the simple flip-chip configuration presented in Figure 1, the input variables to be considered in the experiment have been defined as follows:

- $o$  = conductor overlap
- $w$  = CPW signal line width
- $d$  = distance from bump center to the edge of the ground plane
- $a$  = bump diameter
- $h$  = bump height
- $b$  = substrate thickness

A finite element method (FEM) simulation is performed to test structures similar to the one presented in Figure 1b. The output variable is the magnitude of  $S_{11}$  at 20 GHz. The two levels chosen for each variable are presented in Table 1.

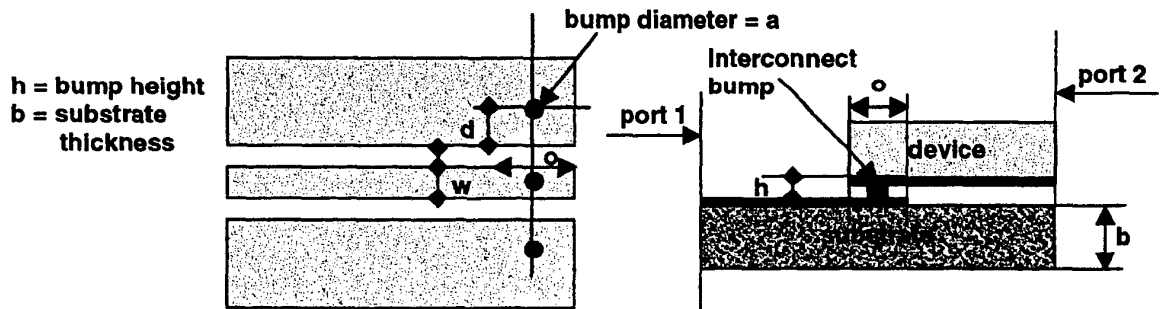


Fig. 1. a) Schematic of the bump configuration.

b) Sideview of the simulated test structure.

	LEVEL -	LEVEL +
A = substrate thickness	10 mil	25 mil
B = CPW signal width	220 $\mu\text{m}$	300 $\mu\text{m}$
C = conductor overlap	300 $\mu\text{m}$	500 $\mu\text{m}$
D = distance from edge of ground plane	50 $\mu\text{m}$	200 $\mu\text{m}$
E = bump diameter	50 $\mu\text{m}$	200 $\mu\text{m}$
F = bump height	25 $\mu\text{m}$	100 $\mu\text{m}$

Table 1.

A  $2^{6-1}$  fractional factorial design was chosen for the 6 variables. The experiment consists of  $2^5 = 32$  treatment combinations, presented in Table 2. The last column shows the value from the

simulated output. A statistical analysis has been performed using SPSS and the results are presented in Table 3.

The highlighted column in Table 3 represents the F statistic for all the 6 input variables and all two-factor interactions. Variables with higher F-values are more statistically significant. The threshold value for statistical significance has been calculated to be 3.2 for this application. Every variable or interaction with an F value higher than 3.2 is considered to be statistically significant. As shown in the table, the highest value of F has been obtained for the conductor overlap (F = 214.091), then bump diameter (F = 39.769) and the CPW signal width (F = 9.080). The substrate thickness has a very low F statistic (0.009), therefore it will be eliminated from further analysis.

Run #	A	B	C	D	E	F=ABCDE	S11@20GHz (dB)
1	-	-	-	-	-	-	-14.1
2	+	-	-	-	-	+	-15.2
3	-	+	-	-	-	+	-14.6
4	+	+	-	-	-	+	-15.1
5	-	-	+	-	-	+	-11.8
6	+	-	+	-	-	+	-10.6
7	-	+	+	-	-	-	-13
8	+	+	+	-	-	+	-12.2
9	-	-	-	+	-	+	-16.5
10	+	-	-	+	-	-	-14.7
11	-	+	-	+	-	-	-15.5
12	+	+	-	+	-	+	-16
13	-	-	+	+	-	-	-12
14	+	-	+	+	-	+	-12.3
15	-	+	+	+	-	+	-11.6
16	+	+	+	+	-	+	-12
17	-	-	-	-	+	+	-12.6
18	+	-	-	+	-	-	-13.8
19	-	+	-	-	+	-	-14.4
20	+	+	-	+	-	+	-13.8
21	-	-	+	-	+	-	-11.5
22	+	-	+	+	-	+	-9.8
23	-	+	+	-	+	+	-10.4
24	+	+	+	+	-	+	-11.4
25	-	-	-	+	+	-	-13.4
26	+	-	-	+	+	+	-13.1
27	-	+	-	+	+	+	-13.2
28	+	+	-	+	+	+	-14.8
29	-	-	+	+	+	+	-9.8
30	+	-	+	+	+	-	-10.8
31	-	+	+	+	+	-	-12.6
32	+	+	+	+	+	+	-11.5

Table 2.

**Tests of Between-Subjects Effects**  
**SPS SFractional Factorial Analysis**

Source	Sum of Squares	df	Mean Square	F	Sig.
Intercept	5369.070	1	5369.070	16580.800	.000
A	2.812E-03	1	2.812E-03	.009	.928
B	2.940	1	2.940	9.080	.013
C	69.325	1	69.325	214.091	.000
D	.945	1	.945	2.919	.118
E	12.878	1	12.878	39.769	.000
F	.945	1	.945	2.919	.118
A * B	.228	1	.228	.704	.421
A * C	.525	1	.525	1.622	.232
A * D	2.531E-02	1	2.531E-02	.078	.785
A * E	.113	1	.113	.348	.568
A * F	1.240	1	1.240	3.830	.079
B * C	9.031E-02	1	9.031E-02	.279	.609
B * D	2.531E-02	1	2.531E-02	.078	.785
B * E	.633	1	.633	1.954	.192
B * F	.945	1	.945	2.919	.118
C * D	9.031E-02	1	9.031E-02	.279	.609
C * E	.750	1	.750	2.317	.159
C * F	.475	1	.475	1.468	.254
D * E	.138	1	.138	.426	.529
D * F	.113	1	.113	.348	.568
E * F	4.133	1	4.133	12.763	.005
Error	3.238	10	.324		

Table 3.

An unexpected result is the statistical insignificance of the bump height, which is known as a very important factor in flip chip design. As mentioned earlier in section 2, all the conclusions are valid only for the specified interval for each variable. Looking at the conductor overlap, the defined interval is between 300 and 500 μm. The large values of the overlap have been imposed by the bump diameter, since the smallest overlap has to be larger than the largest diameter. The parasitic capacitance of the interconnection is due to both overlap and bump height. In the case of the large overlap, it can be assumed that all the parasitic capacitive effect is due to the overlap and the bump height becomes insignificant. Therefore, further bump height analysis has been performed for a lower value of the overlap. Three values for the bump height: 25 μm, 60 μm and 100 μm have been combined with a 120 μm overlap. The other variables have been chosen as follows: distance to the

edge of the ground plane = 50  $\mu\text{m}$ ; CPW width = 220  $\mu\text{m}$ , and bump diameter = 50  $\mu\text{m}$ . The result of the simulated  $|S_{11}|$  at 20 GHz versus bump height is presented in Figure 2.

The variation is more than 4 dB, and the comparison with the variation of the output for the entire experiment (Table 2) of maximum 6.7 dB, shows that the bump height is a significant factor for smaller values of the overlap.

A very important step in the validation of the statistical model is the linearity check, usually done by designing an extra center point. No center point has been considered for this particular experiment, however linearity can be checked. In the case of the conductor overlap, the additional analysis for the bump height provided the third point in the variation of the output with the respective variable. The plot of  $|S_{11}|$  at 20 GHz with the overlap is presented in Figure 3 and it shows a linear variation.

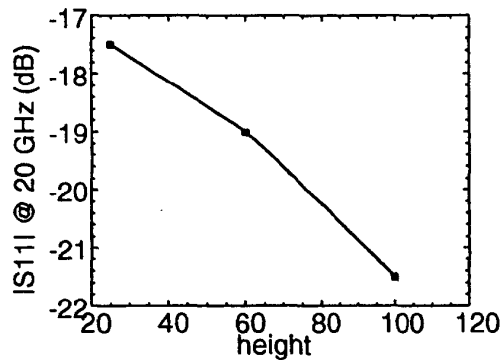


Fig. 2. Variation with bump height

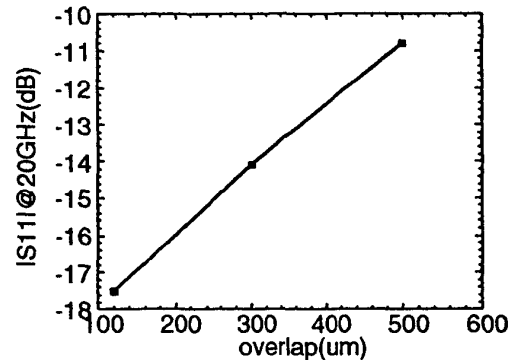


Fig. 3. Linearity check for the conductor overlap

#### 4. Conclusion

A novel approach for flip-chip design rule development has been presented. The method is based on properly designing a fractional factorial experiment and statistically analyzing the output. The variables found to be the most significant are the conductor overlap, bump diameter and CPW signal width. The substrate thickness is not significant and it can be eliminated from the analysis. The bump height is not significant for large overlaps, but becomes significant for smaller and therefore more practical overlap values. The FEM simulation results have been used for designing a set of test structures currently under fabrication. The method is very flexible and will be extended to measurement data, used to both validate the presented method and evaluate the repeatability of the fabrication process. A regression model will be developed and applied to scale the lumped element values in an equivalent circuit model of the bump transition, for developing design rules and technical insight for flip chip interconnections at RF and microwave frequencies.

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