Coupling Between Microstrip Lines Embedded in Polyimide Layers for 3D-MMICs on Si

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Abstract — **Three-dimensional circuits built upon multiple layers of polyimide are required for constructing Si/SiGe monolithic microwave/millimeter-wave integrated circuits on CMOS (low resistivity) Si wafers. However, the closely spaced transmission lines are susceptible to high levels of coupling, which degrades circuit performance. In this paper, Finite Difference Time Domain (FDTD) analysis and measured characteristics of novel shielding structures that significantly reduce coupling between embedded microstrip lines are presented.**

I. INTRODUCTION

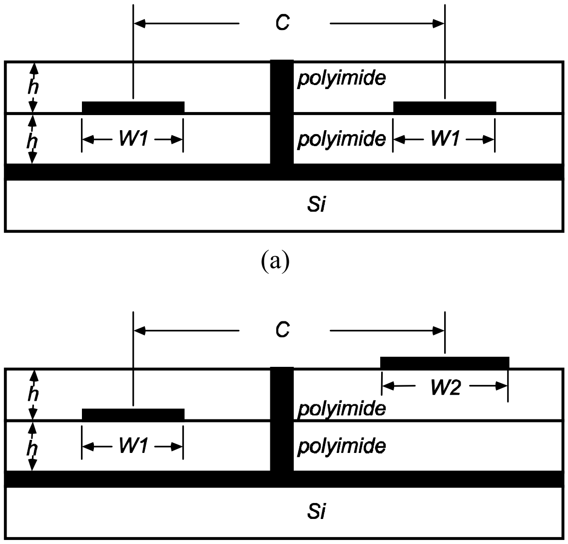
There is a rapidly expanding market for Si Microwave/Millimeter-Wave Integrated Circuits (MMICs) fabricated in standard CMOS foundries to replace GaAs MMICs in wireless communication systems, phased array radar, and other applications where the circuit cost is a major factor in determining the system cost. However, microwave passive elements and transmission lines placed directly on standard CMOS grade Si have low quality factors (high attenuation), which necessitates novel transmission line structures [1] that are typically embedded in polyimide that is deposited over the Si substrate. Moreover, highly integrated systems that include the RF circuits, digital data processing circuits, and bias control circuits on a single chip or within a single package also rely on multiple layers of polyimide to construct three-dimensional circuits that are smaller than what would normally be possible.

Although thin film microstrip (TFMS) embedded in polyimide solve the problem of high attenuation and smaller sized circuits, closely spaced transmission lines also increases the potential for high levels of coupling between lines. If the interline crosstalk is too high, the circuit characteristics are severely degraded. Thus, techniques and layout rules are required to reduce coupling between parallel TFMS lines. Prior papers on reducing coupling between microstrip lines built on Low Temperature Cofired Ceramic (LTCC) have shown that a roll of via holes placed between the two lines reduces coupling by 8 dB if the via holes are connected on the top and bottom by a strip and the ground plane respectively [2]. A continuous metal filled wall fabricated between two TFMS lines embedded within polyimide has been shown to also reduce coupling by approximately 8 dB for a single microstrip geometry [3].

In this paper, a systematic evaluation of the coupling between TFMS lines embedded in polyimide built upon CMOS grade Si is presented for the first time. This in depth characterization includes a comparison between the use of metal filled via hole fences and metal walls embedded in the polyimide to reduce coupling. To characterize the coupling, Finite Difference Time Domain (FDTD) and measurements are used.

II. CIRCUIT DESCRIPTION

Figure 1 shows a cross sectional cut through microstrip lines embedded in polyimide upon a Si substrate. The microstrip ground plane covers the Si substrate, which shields all of the electromagnetic fields from the lossy Si. W1 and W2 are 23 μm and 52 μm respectively to yield a 50 Ω transmission line for the polyimide thickness, h, of 10 μm. Several shielding structures between the two microstrip lines are characterized. For microstrip lines on the same polyimide layer as shown in Figure 1a, the shielding structures are: a roll of metal filled via holes through polyimide layer 1 only, a roll of metal filled via holes through both layers of polyimide, and a continuous, metal filled trench through both layers of polyimide. For microstrip lines on different layers of polyimide as shown in Figure 1b, the shielding structures are a roll of metal filled via holes through both layers of polyimide and a metal filled trench through both layers of polyimide. In all cases, the via holes are 20 by 20 μm and circuits are analyzed with the via hole spacing, DV, of 60 and 100 μm from center to center. Furthermore, all via holes are connected by a continuous, 20 μm wide metal strip as recommended in [2]. The metal filled trench is 20 μm wide.



(a)

(b)

Figure 1: Cross sectional cuts through microstrip lines embedded in polyimide layers with a shielding structure between them. (a) microstrip lines on same layer of polyimide and (b) microstrip lines on different layers of polyimide.

The circuit for characterizing coupling between the microstrip lines is shown in Figure 2. The four-port circuit has probe pads orientated so that each port may be probed simultaneously. The coupling region, or the section of parallel transmission lines labeled L in Figure 2, is 5000 μm long. Note that for characterization, the shielding structure extends past the transmission line right angle bend and is tapered at 45 degree to minimize the effects of radiation from the right angle bend.

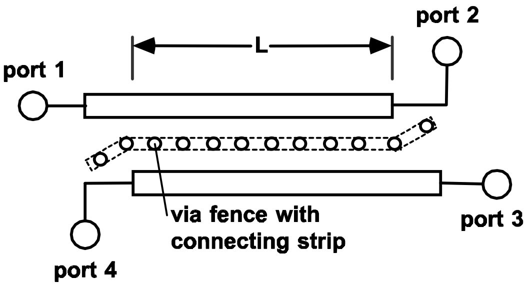


Figure 2: Schematic of the coupled line structures used to characterize the coupling.

II. THEORETICAL ANALYSIS

The full-wave FDTD technique [4] is used for the theoretical characterization of the forward and backward coupling, S_{31} and S_{41} respectively, between the two parallel microstrip lines. The E- and H-field components are implemented in a leapfrog configuration. An adaptive grid with neighboring cell aspect ratio smaller or equal to 2 maintains a second-order global accuracy.

Numerical meshes of 80-120 by 45 by 250 cells terminated with 10 Perfectly Matched Layer (PML) cells in each direction provide accurate results for a time-step of $\Delta t=0.99\Delta t_{max}$. A Gaussian pulse with f_{max}=60GHz is applied vertically as a soft source close to the front end of the microstrip, and its values get superimposed on the FDTD calculated field value for all cells in the excitation region for each time-step. The via holes are modeled as rectangular metal tubes with cross-section 23x20 μm. To account for the coupling of even and odd modes, two simulations are performed for each geometry exciting both lines with equal amplitude and even or odd space distributions respectively. In addition, both microstrip lines are terminated with matched loads (Z_o=50 Ω) that are realized as the combination of shunt resistors placed between the microstrip and the bottom ground [5]. Two probes placed at the front end and at the far end of one line are used for the combination of the results of the even and of the odd simulations. The application of the FFT algorithm derives the frequency-domain results from the time-domain data (usually 25,000 time-steps).

III. CIRCUIT FABRICATION AND CHARACTERIZATION

The four port microstrip circuits are fabricated on a 1 Ω-cm Si wafer. A ground plane consisting of a 300 Å Ti adhesion layer, 1.5 μm of Au, and a 200 Å Cr cap layer is first evaporated onto the Si wafer. This is followed by spinning on Dupont adhesion promoter and 10 μm of Dupont PI-2611 polyimide, which has a permittivity of 3.12 measured at 1 MHz [6] and a loss tangent of 0.002 measured at 1 kHz [7]. After curing the polyimide at 340 C for 120 minutes, Ni is evaporated onto the polyimide to serve as a mask for the O_2/CF_4 reactive ion etching (RIE) of the via holes. After the via holes are etched and the Ni removed, 200 Å of Ti and 2000 Å of Au are sputtered onto the wafer to serve as a seed layer for the 1.3 μm of Au electroplating that is used to define the embedded microstrip lines and fill the via holes in a single step. This Au is capped with 200 Å of Cr before applying the next layer of polyimide. Thus, all metal structures are 1.5 μm thick. This process is repeated for each layer of polyimide. After each step, a DEKTAK surface profile is used to measure the polyimide and metal strip thickness. Both, the DEKTAK and SEM analysis show that the surface roughness is low enough that it can be neglected in the analysis.

Measurements are made on a vector network analyzer from 2 to 50 GHz. A Thru/Reflect/Line (TRL) calibration is implemented with MULTICAL [8], a TRL software program, using four delay lines of 1800, 2400, 4800, and 10000 µm and a short circuit reflect fabricated on the same substrate as the circuits. To improve accuracy, each circuit is measured several times and the average of those measurements is presented in this paper. During the measurement of the four-port circuits, two of the four ports are terminated in 50 Ω loads built into especially designed RF probes.

III. MICROSTRIP COUPLING RESULTS

As a first step, the measured and FDTD analysis results for the embedded microstrip lines are compared across the entire frequency band of 2 to 50 GHz. One such case for coupled microstrip lines without any shielding structure is shown in Figure 3. It is seen that there is excellent agreement between the theory and the measured results, which is typical of the other cases. Also typical of all of the results presented in this paper, the forward coupling, S_{31}, increases monotonically with frequency, while the backward coupling, S_{41}, is periodic. Thus, throughout the paper, the backward coupling results presented are the maximum coupling value over the frequency band.

The effect of shielding structures on the coupling level between parallel microstrip lines fabricated on the same layer, as shown in Figure 1a, is summarized in Figure 4. Presented results are backward coupling defined as $-20*\log|S_{41}|$ and forward coupling defined as $-20*\log|S_{31}|$. First, note the excellent agreement between measured and FDTD results for all structures. Second, it is seen that for closely spaced lines without any via hole structures, the coupling is very high (approximately 30 dB), but that the coupling decreases as C increases to approximately 45 dB. Third, it is seen that a shielding structure only in layer 1 offers very little help in lowering the coupling, but that the roll of via holes through both layers of polyimide (layer 2) and the metal filled trench greatly reduce coupling. Fourth, the via fence interconnected by a metal strip yields the same coupling level as the metal filled trench for C greater than 80 µm; however, for closer spaced lines, the trench provides better shielding for the forward coupling. The backward coupling is reduced by approximately 15 dB and the forward coupling is reduced by approximately 10 dB at 25 GHz for closely spaced lines. Moreover, it is seen that the use of shielding structures enables microstrip transmission lines to be placed as close as 60 µm while yielding the same coupling as lines with no shielding structures placed 130 µm apart. Lastly, although not shown, it was found that the results are not dependent on the via hole spacing (DV= 60 or 100 µm).

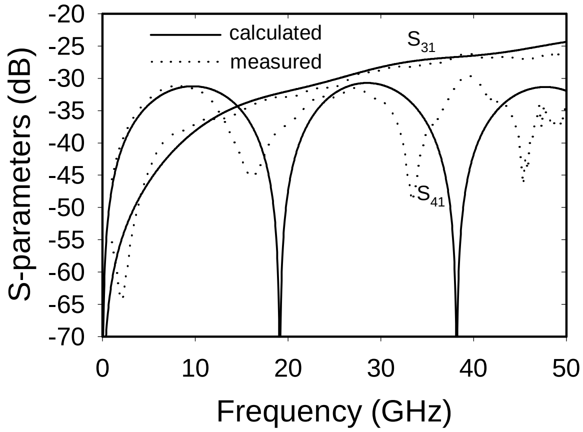
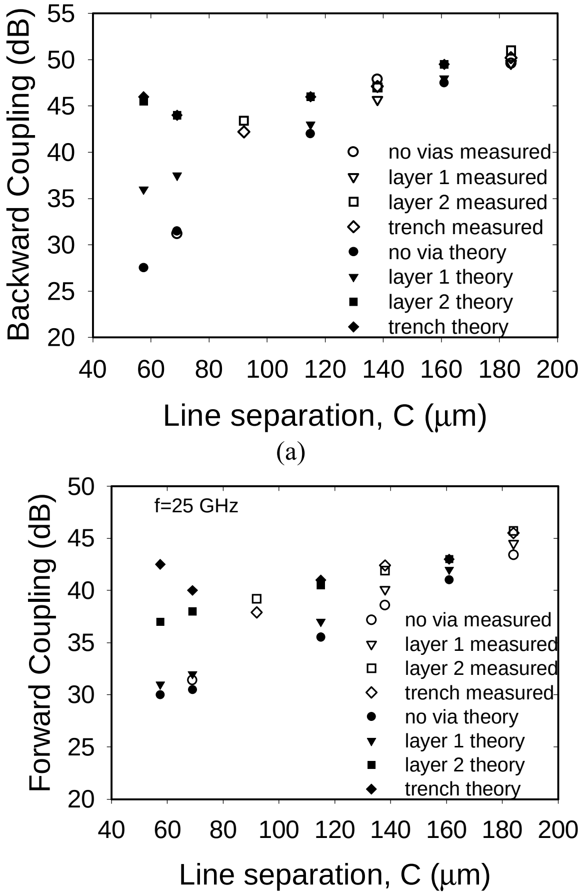


Figure 3: Comparison of measured and FDTD scattering parameters for coupled microstrip lines on the same polyimide layer (Figure 1a) with no shielding structure and C=69 µm.

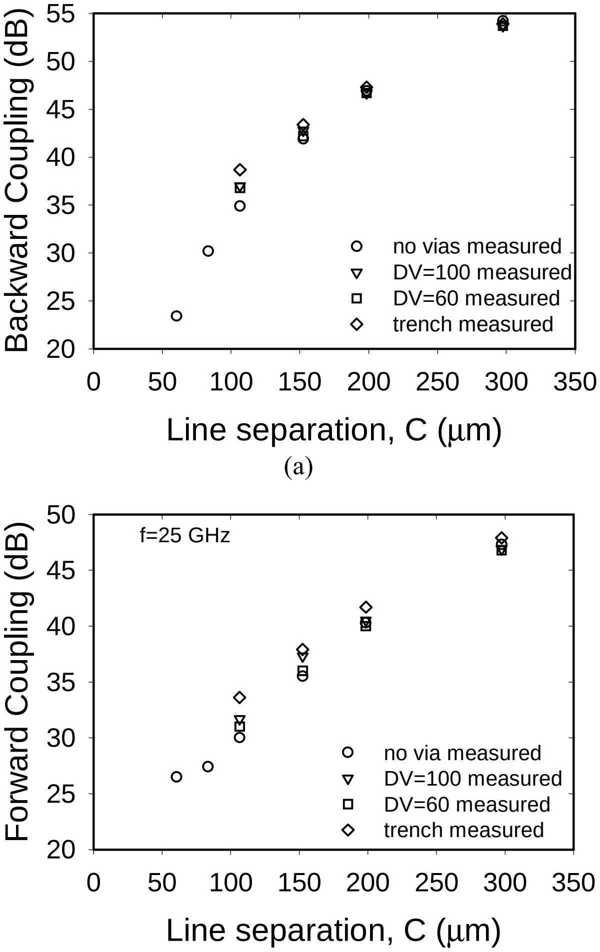


(b)

Figure 4: Measured and FDTD (a) backward coupling and (b) forward coupling of microstrip lines fabricated on the same layer of polyimide (Figure 1a) as a function of center to center spacing, C.

The measured coupling between microstrip lines fabricated on different layers of polyimide as shown in

Figure 1b are summarized in Figure 5. Generally, the observations pertaining to Figure 4 are true here as well, but the reduction in coupling with shielding structures is very small, approximately 5 dB.



(a)

(b)

Figure 5: Measured (a) backward coupling and (b) forward coupling of microstrip lines fabricated on different layers of polyimide (Figure 1b) as a function of center to center spacing, C.

Comparing the two different cases shown in Figures 4 and 5, it is seen that microstrip lines embedded on the same layer of polyimide with shielding structures that extend to the top of polyimide have approximately 10 dB less coupling than microstrip lines on different layers with the same shielding structure. Thus, while it may be necessary to place microstrip transmission lines on different layers of polyimide to reduce circuit size, this will result in higher coupling.

V. CONCLUSION

In this paper, a systematic evaluation of shielding structures for reducing coupling between microstrip lines embedded in polyimide has been presented. The results show that coupling is lower when both microstrip lines are on the same layer of polyimide and when the shielding structure extends through both layers of polyimide. For closely spaced microstrip lines, coupling is lower for a metal filled trench shield than via fences connected with a metal strip; however, for wider spaced lines, there is no difference in coupling between via fences and metal wall shields.

REFERENCES

[1] G. E. Ponchak, “RF transmission lines on silicon substrates,” *29 th European Microwave Conference Dig.*, Munich, Germany, Oct. 5-7, 1999, pp. 158-161.
[2] G. E. Ponchak, D. Chun, J.-G. Yook, and L. P. B. Katehi, “The use of metal filled via holes for improving isolation in LTCC RF and wireless multichip packages,” *IEEE Trans. on Advanced Packaging*, Vol. 23, No. 1, pp. 88-99, Feb. 2000.
[3] K. Onodera, M. Hirano, M. Tokumitsu, I. Toyoda, K. Nishikawa, and T. Tokumitsu, “Folded U-shaped microwave technology for ultra-compact three-dimensional MMIC’s,” *IEEE Trans. Microwave Theory Tech.*, Vol. 44, No. 12, pp. 2347-2353, Dec. 1996.
[4] A. Taflove, *Computational Electrodynamics*, Artech House, Dedham, MA, 1995.
[5] L.Roselli, E.Tentzeris and L.P.B.Katehi, “Nonilnear circuit characterization using a multiresolution time domain technique,” *Proc. of the 1998 MTT-S Conference*, pp.1387-1390, Baltimore, MD.
[6] J. Leu, H.-M. Ho, J. K. Lee, J. Kasthurirangan, C. N. Liao, and P. S. Ho, “The evaluation of low dielectric constant materials for deep submicron interconnect applications,” in *Proc. 6th Meeting Dupont Symp. Polyimide Microelectronics*, May 1-3, 1995.
[7] Dupont Company Pyralin LX data sheet.
[8] R. B. Marks, “A multilane method of network analyzer calibration,” IEEE Trans. Microwave Theory Tech., Vol. 39, pp. 1205-1215, July 1991.