MULTI-LAYER 3D SYSTEM-ON-PACKAGE (SOP) ARCHITECTURES FOR HIGHLY INTEGRATED MICROWAVE AND MILLIMETER WAVE RADIO FRONT-END

J. Laskar, A. Sutono*, D. Staiculescu*, C.–H. Lee*, M.F. Davis, K. Lim, and M.Tentzeris
Packaging Research Center
School of ECE
Georgia Institute of Technology
Yamacraw Design Center
Atlanta, GA 30332, USA;
*Now with RF-Solutions Inc., Atlanta, GA, 30309, USA
dstaiculescu@rf-solutions.com

ABSTRACT

This paper summarizes the development of compact and highly integrated microwave and millimeter wave radio front-end System-on-Package (SOP). The three-dimensional transceiver front-end SOP architectures incorporate on-package integrated lumped element passives as well as RF functions primarily filters, baluns, and antennas in standard multi-layer LTCC and fully-organic technologies. In addition, the use of flip-chip technology for attaching the MMIC to the module can improve the electrical performance to frequencies as high as 75 GHz, increases the integration level and reduces assembly time and cost. These prototypes suggest the feasibility to develop highly miniaturized cost-effective SOP transceiver applicable not only for wireless applications but also for high-speed optoelectronics links.

Key words: System-on-package, flip chip, embedded filter.

INTRODUCTION

The current drawbacks of most commercially available microwave and millimeter wave front-ends, such as the Ku-band satellite transceivers for outdoor units, are their relatively large size and heavy weight primarily caused by discrete components such as the filters, and separately located modules [1]. Multi-layer ceramic and organic-based SOP implementation are capable of overcoming this limitation by integrating components as part of the module package that would have otherwise been acquired in discrete form. On-package components not only miniaturize the module, but also eliminate or minimize the need for discrete components and thereby reduce the assembly time and cost. In addition, the use of vertical interconnects such as flip chip contributes to higher integration and the compatibility with automatic manufacturing reduces the assembly time and cost as well. In this paper, we demonstrate a C-band LTCC-stripline filter performance incorporated in a 5.8 GHz radio module. Also, an original method for the optimization of the flip chip assembly is presented and applied to a simple CPW to CPW transition with measured return loss results better than 17 dB to as high as 75 GHz.

LTCC AND FULLY-ORGANIC BASED ARCHITECTURES

Figures 1 and 2 illustrate a transceiver topology optimized for multi-layer ceramic and organic, respectively.

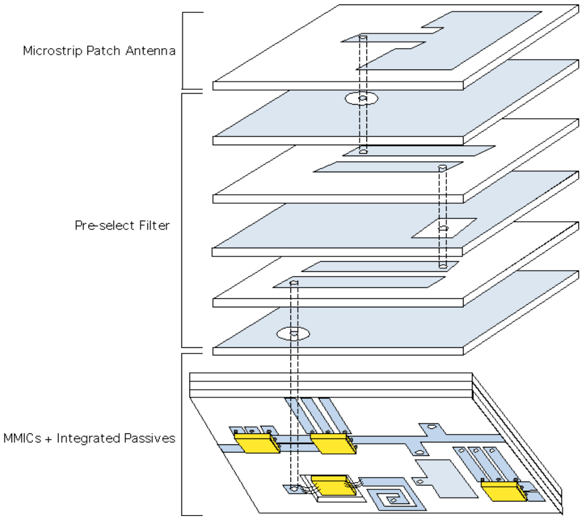

Figure 1. SOP-based integrated RF front-end optimized for multi-layer ceramic-based technologies.

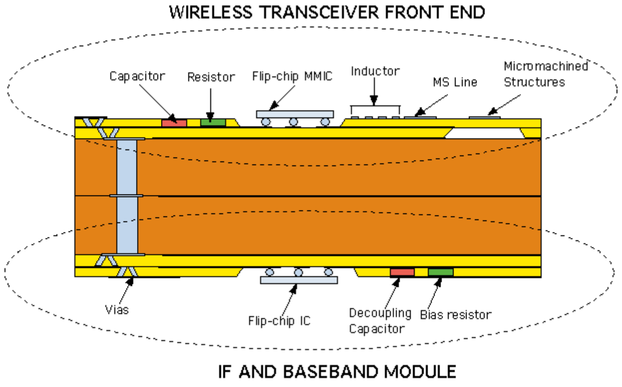

Figure 2. SOP-based integrated RF front-end optimized for multi-layer organic-based technologies.

The topology depicted in Figure 1 can be implemented in LTCC or HTCC technologies while that in Figure 2 is applicable for example, in Georgia Tech's PRC fully organic process incorporating double sided FR-4 board laminated with two organic materials on which passive components are integrated [2]. Low loss transmission line performance has been demonstrated for this technology. The SLIM process consists of a FR-4 base substrate laminated with two layers of Dupont's Vialux™ materials. The first layer laminated directly on the surface of the FR-4 board is 2 mils thick while the second layer is one mil thick. Flip chip and bond-wire attachment techniques were utilized to attach IC chips to the board. A cross sectional view of a complete transceiver including the IF and baseband modules is shown in Figure 2. The double-sided SLIM board is divided evenly to deploy RF components on the top side and the IF-baseband components on the bottom side.

Two hybrid-coplanar waveguide and microstrip interconnect schemes have been proposed [2]. In the first scheme, coplanar waveguide (CPW) transmission lines are fabricated on the FR-4 board to allow MMICs to be attached through a flip-chip process. Microstrip interconnects utilizing both grounds of the CPW lines are established on the laminant layer through a via transitioning from the CPW to the microstrip signal lines. An alternative interconnect scheme is where the CPW lines are fabricated on the first laminant layer with the surface of the FR-4 board fully metalized. Such a configuration potentially improves the interconnect performance since the CPW lines are fabricated on a thinner layer with a better loss performance than FR-4.

Figure 3 shows an example of the PRC-SOP test coupon consisting of transmission lines, transitions, inductors, capacitors and antennas.

The inductors incorporate novel hollow and patterned ground plane configurations to reduce the eddy current flow and thereby improving the Q and the resonant frequency. The filters and antennas have been designed in compact microstrip and stripline as well as slotline configurations for L and C-band wireless applications.

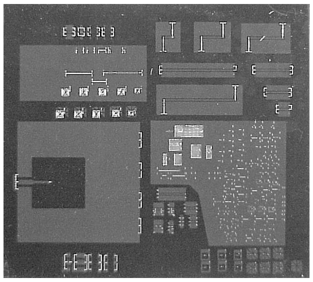

Figure 3. An example of PRC-organic SOP test board containing transmission lines, transitions, inductors, capacitors and antenna.

The ceramic-based RF front-end real-estate allocation in Figure 1 deploys the antenna on the uppermost layer which can be conveniently implemented in microstrip patch, dipole and brickwall arrays to provide adequate gain. Two stripline filter topologies inserted between the antenna and the rest of the radio front-end system on the back side of the assembly where MMIC chips are attached along with other integrated passives have been developed and fully characterized at L, C and Ku-band [3,4,5]. The antenna's vertical feed connecting through the microstrip ground plane not only serves as its interface to the filter input, but also as an important part of the input matching of the antenna. The filter output is vertically connected to the rest of the module shown in the bottom portion in Figure 1 consisting of Monolithic Microwave Integrated Circuit (MMIC) chips and on-board integrated passive components. There are two popular MMIC attachment options to the board: bond wires on chip dropped in a cavity to ensure a short electrical path and minimize parasitics, and flip chip bumps; both are shown in Figure 1. The availability of additional dielectric layers make it possible for the three-dimensional deployment of other integrated passives such as baluns, lumped inductors, capacitors, and resistors, as well as IF or low pass filters, for example, in the case of a superheterodyne or direct conversion scheme, respectively. Another example is the integrated balun which can be interfaced to a push-pull power amplifier or a mixer. The input matching of a low noise amplifier or input and output matching of a power amplifier typically done by discrete passives can be conveniently replaced by their on-board integrated version.

Figure 4 plots the C-band LTCC-stripline filter performance incorporated in a 5.8 GHz radio module [5].

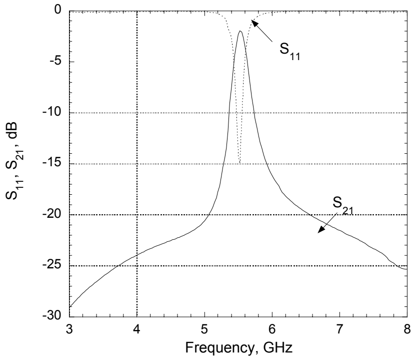

Figure 4. Measured performance of a C-band LTCC embedded stripline filter.

This filter exhibits a measured insertion loss of less than 2 dB at 5.5 GHz and narrowband performance of 200 MHz suitable for IEEE 802.11 WLAN. In addition, the C-band LTCC filter also exhibits not only superior in performance but also due to the fact that this filter can be embedded , to a similar filter fabricated in MCM-D technology [6] at 5.2 GHz which exhibits a bandwidth over 500 MHz. LTCC component library have also been established and incorporated in the1.9 GHz and 2.4 GHz CMOS power amplifier modules yielding 27dBm and 24 dBm output power [7-8] and over 45% efficiency have been demonstrated. The 1.9 GHz PA is for DECT application while the 2.4 GHz PA is suitable to provide Bluetooth power level 1 to cover transmission range as far as 100m. These demonstration vehicles are the first reported CMOS PAs with fully integrated LTCC integrated passives.

The need for vertical integration and better interconnect performance with increased frequency applications makes the flip chip the potential technology of choice. The transition performance to 75 GHz is optimized using a design of experiments method. This has been used before for RF and microwave flip-chip design rule development [9]. Two known optimization methods, signal bump misalignment [10] and transmission line compensation [11] are combined together in an experiment to study how they affect together the assembly performance and what is the optimal combination between them in a certain range of values. Schematics of the two methods are presented in Figure 5.

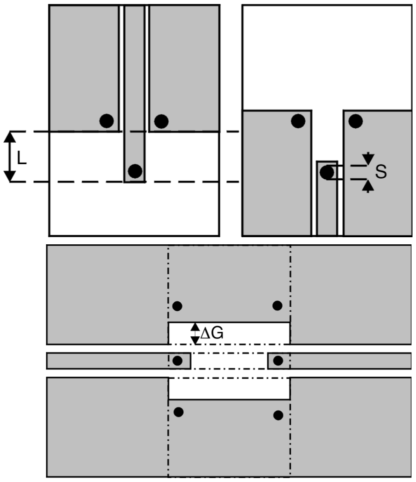

Figure 5. Two optimization techniques: signal staggering and transmission line compensation

For frequencies higher than 30 GHz, individual analysis shows that the signal bump misalignment dramatically improves the return loss performance, while the transmission line compensation degrades it. When combined together in a factorial experiment, it has been found out that the optimal structure has minimum misalignment and maximum compensation. This is due to the strong interaction between the two and it is a result that couldn't have been predicted using a one-at-a-time analysis method. The measured performance of the optimal structure from 1 to 75 GHz is presented in Figure 6.

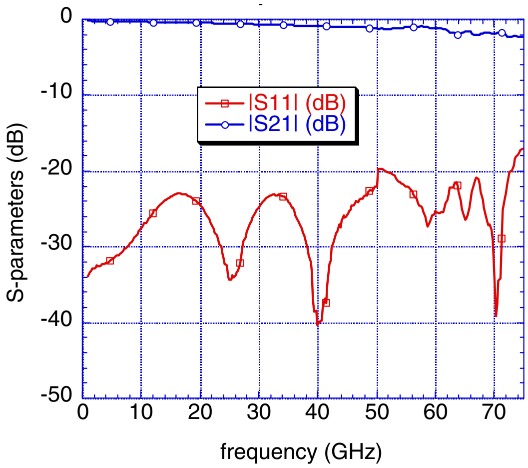

Figure 6. Measured S-parameters of optimized structure

CONCLUSION

Compact and highly integrated SOP RF technologies have been proposed and demonstrated for various applications in ceramic and organic technologies for various applications. On-package components in addition to the use of vertical interconnections such as flip-chip not only reduce cost but also allow a tremendous miniaturization of the assembly that address the demand and specifications for portability and light weight. These prototypes suggest the feasibility to develop highly miniaturized cost-effective SOP transceiver, which can be applied not only for wireless applications but also for optoelectronics links.

ACKNOWLEDGEMENT

The authors would like to acknowledge the support of the NSF Packaging Research Center at Georgia Tech, the Yamacraw Design Center and the NSF Career Award. We also would like to thank National Semiconductor for fabricating the LTCC prototypes and Rockwell Collins for fabricating the flip-chip prototypes.

REFERENCES

[1] J.W. Gipprich, L.E. Dickens, J.A. Faulkner, “Power amplifier yields 10 watts over 8-14 GHz using GaAs MMICs in an LTCC serial combiner/divider network,” Proceedings of IEEE IMS, Atlanta, GA, 1993, pp. 1369-1372.

[2] M.F. Davis, A. Sutono, K Lim, J. Laskar, and R. Tumamala, “Multi-layer fully organic based System on Package (SOP) technology for RF applications”, Proceedings of IEEE EPEP, Scottsdale, AZ, 2000, pp103-106.

[3] C.-H. Lee, A. Sutono, S. Han, J. Laskar, “A compact LTCC Ku-band transmitter module with integrated filter for satellite communication applications,” Proceedings of IEEE IMS, Phoenix, AZ, 2001, pp.945-948.

[4] A. Sutono, J. Laskar, and W.R. Smith, "Development of three dimensional integrated bluetooth image reject filter," Proceedings of IEEE-IMS, Boston, MA, 2000, pp. 339-342.

[5] K.Lim, A. Obatoyinbo, A. Sutono, S. Chakraborty, C. Lee, E. Gebara, A. Raghavan, J. Laskar,"A highly integrated transceiver module for 5.8 GHz OFDM communication system using multi-layer packaging technology," Proceedings of IEEE-IMS, Phoenix, AZ, 2001.

[6] S. Donnay; P. Pieters; K. Vaesen.; W. Diels.; P. Wambacq.; W. De Raedt.; E. Beyne.; M. Engels.; I. Bolsens, .” Chip-package codesign of a low-power 5-GHz RF front end”, Proceedings of the IEEE, vol. 88, no.10, pp. 1583-1597.

[7] A. Sutono, D.Heo, E.Chen, J. Laskar, W.R. Smith, "Compact implementation of component library in LTCC technology and its applications to CMOS RF power amplifier design", Proceedings of IEEE EPEP, Scottsdale, AZ, 2000, pp.288-291.

[8] D. Heo, A. Sutono, Y.Suh, E. Gebara, E. T-K. Dalton, J. Laskar, E. Tentzeris, "A high efficiency 0.25-um CMOS PA with LTCC multi-layer high-Q integrated passives for 2.4 GHz ISM band", *Proceedings of IEEE-IMS,* Phoenix, AZ, 2001.

[9] D. Staiculescu, J. Laskar, E.M. Tentzeris, “Design rule development for microwave flip-chip applications”, IEEE Trans. Microwave Theory Tech., vol. 48, no. 9, September 2000, pp. 1476-1481.

[10] H.H.M. Ghouz, EL-Badawy EL-Sharawy, “Finite-difference time-domain analysis in flip-chip interconnects with staggered bumps”, IEEE Trans. Microwave Theory Tech., vol. 44, no. 6, June 1996, pp. 960-963.

[11] N. Iwasaki, F. Ishitsuka, K. Kato, “High performance flip-chip technique for wide-band modules”, Proceedings of IEEE EPEP, Napa, CA, 1996, pp. 207-209.